

BIPOLAR JUNCTION TRANSISTOR WITH A SELF-ALIGNED EMITTER AND BASE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a divisional of application Ser. No. 13/042,902, filed Mar. 8, 2011, which is hereby incorporated by reference herein in its entirety.

BACKGROUND

The invention relates generally to semiconductor device fabrication and, in particular, to bipolar junction transistors with a self-aligned emitter and base, as well as fabrication methods for bipolar junction transistors and design structures for BiCMOS integrated circuits.

Bipolar junction transistors are typically found in demanding types of analog circuits, especially analog circuits used in high-frequency applications. Bipolar junction transistors are found in radiofrequency integrated circuits (RFICs) used in wireless communications systems, as well as integrated circuits requiring high power efficiency, such as power amplifiers in cellular telephones, and other types of high speed integrated circuits. Bipolar junction transistors may be combined with complementary metal-oxide-semiconductor (CMOS) field effect transistors in bipolar complementary metal-oxide-semiconductor (BiCMOS) integrated circuits, which take advantage of the favorable characteristics of both transistor types.

Conventional bipolar junction transistors include three semiconductor regions, namely the emitter, base, and collector regions. Generally, a bipolar junction transistor includes a pair of p-n junctions, namely an emitter-base junction and a collector-base junction. A bipolar junction transistor (HBT) is a variety of bipolar junction transistor that employs at least two semiconductor materials with unequal band gaps for the emitter and base regions, creating a heterojunction. For example, the base of a HBT may be comprised of silicon germanium (SiGe), which is characterized by a narrower band gap than silicon typically composing the emitter of the HBT.

Improved devices are needed for HBT's that boost device performance, as well as improved fabrication methods for HBT's and design structures for BiCMOS integrated circuits.

BRIEF SUMMARY

In an embodiment of the invention, a method is provided for fabricating a bipolar junction transistor. The method includes forming an intrinsic base layer, forming a sacrificial mandrel on a top surface of the intrinsic base layer, and forming an extrinsic base layer on the top surface of the intrinsic base layer. The extrinsic base layer is self-aligned with the sacrificial mandrel. The method further includes partially removing the sacrificial mandrel to define an emitter window to the top surface of the intrinsic base layer and forming an emitter in the emitter window that contacts the top surface of the intrinsic base layer.

In an embodiment of the invention, a method is provided for fabricating a bipolar junction transistor. The method includes forming trench isolation regions in the semiconductor substrate that surround a device region of a semiconductor substrate. A monocrystalline raised region of an intrinsic base layer is formed over the device region of the substrate. A polycrystalline region of the intrinsic base layer is formed over the trench isolation regions. The polycrystalline region

includes a first sections and second sections of a lesser thickness than the first sections. The method further includes epitaxially growing an extrinsic base layer on a top surface of the intrinsic base layer using a selective epitaxial growth process.

A portion of the extrinsic base layer is selectively grown on the polycrystalline region of the intrinsic base layer and fills open spaces between the second sections of the polycrystalline region that the polycrystalline region has a substantially planar top surface.

In an embodiment of the invention, a device structure for a bipolar junction transistor includes an intrinsic base and an extrinsic base on the top surface of the intrinsic base. An emitter window extends through extrinsic base and to a raised region of the intrinsic base. Spacers line the emitter window. An emitter is in contact with the intrinsic base. The emitter is disposed in the emitter window and separated from the extrinsic base by the spacers. The spacers lining the emitter window function to self-align the extrinsic base with the emitter.

In an embodiment of the invention, a hardware description language (HDL) design structure is encoded on a machine-readable data storage medium. The HDL design structure comprises elements that, when processed in a computer-aided design system, generates a machine-executable representation of a bipolar junction transistor. The HDL design structure includes an intrinsic base and an extrinsic base on the top surface of the intrinsic base. An emitter window extends through extrinsic base and to a raised region of the intrinsic base. Spacers line the emitter window. An emitter is in contact with the intrinsic base. The emitter is disposed in the emitter window and separated from the extrinsic base by the spacers. The spacers lining the emitter window function to self-align the extrinsic base with the emitter. The HDL design structure may comprise a netlist. The HDL design structure may also reside on storage medium as a data format used for the exchange of layout data of integrated circuits. The HDL design structure may reside in a programmable gate array.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate various embodiments of the invention and, together with a general description of the invention given above and the detailed description of the embodiments given below, serve to explain the embodiments of the invention.

FIGS. 1-9 are cross-sectional views of a portion of a substrate at successive fabrication stages of a processing method for fabricating a device structure in accordance with an embodiment of the invention.

FIG. 3A is a detailed view of a portion of FIG. 3 after the extrinsic base layer is formed.

FIG. 3B is a detailed view similar to FIG. 3A before the extrinsic base layer is formed.

FIGS. 6A and 6B are cross-sectional views similar to FIG. 6 in accordance with alternative embodiments of the invention.

FIGS. 10-12 are cross-sectional views of a portion of a substrate at successive fabrication stages of a processing method for fabricating a device structure in accordance with an alternative embodiment of the invention.

FIGS. 13-17 are cross-sectional views of a portion of a substrate at successive fabrication stages of a processing method for fabricating a device structure in accordance with an alternative embodiment of the invention.